Synchronous DRAM

1M x 16 Bit x 4 Banks CS56ES64163

■ DESCRIPTION

The CS56ES64163 is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 1,048,576 words by16 bits. Synchronous design allows precise cycle controls with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable device to be useful for a variety of high bandwidth, high performance memory system applications.

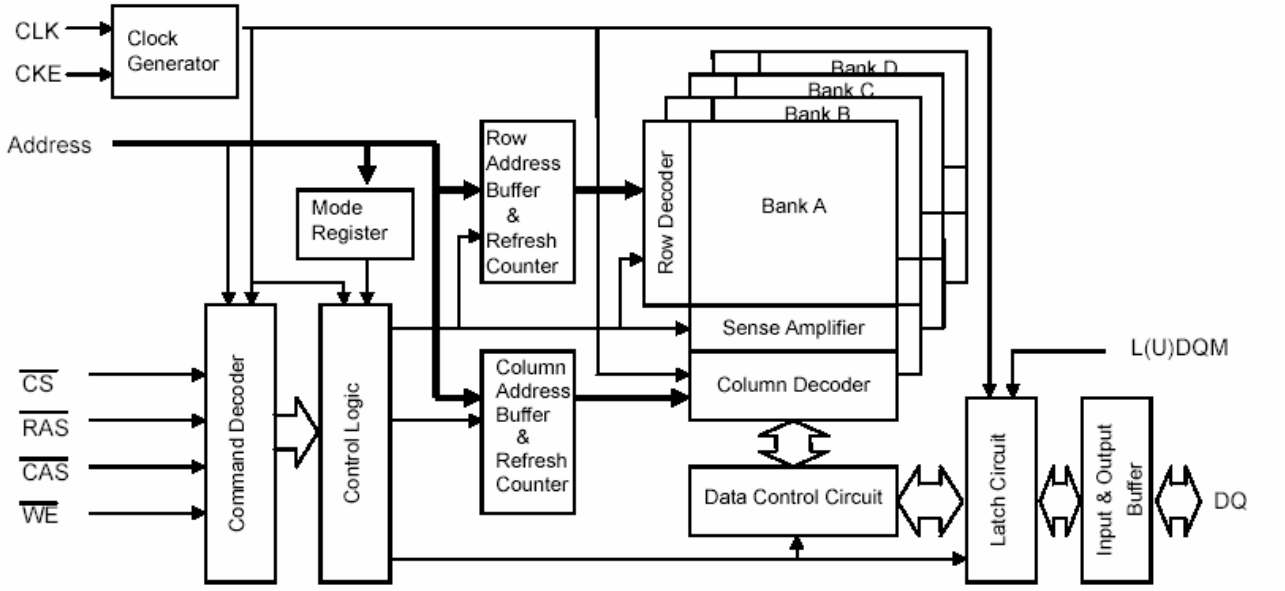
■ FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - CAS Latency (2 & 3)
  - Burst Length (1, 2, 4, 8 & full page)
  - Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

■ PIN ASSIGNMENT

Pin No.	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
Pin Name	VDD	DQ0	VDDQ	DQ1	DQ2	VSSQ	DQ3	DQ4	VDDQ
Pin No.	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**
Pin Name	DQ5	DQ6	VSSQ	DQ7	VDD	LDQM	/WE	/CAS	/RAS
Pin No.	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**
Pin Name	/CS	A13	A12	A10/AP	A0	A1	A2	A3	VDD
Pin No.	**28**	**29**	**30**	**31**	**32**	**33**	**34**	**35**	**36**
Pin Name	VSS	A4	A5	A6	A7	A8	A9	A11	NC
Pin No.	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**
Pin Name	CKE	CLK	UDQM	NC	VSS	DQ8	VDDQ	DQ9	DQ10
Pin No.	**46**	**47**	**48**	**49**	**50**	**51**	**52**	**53**	**54**
Pin Name	VSSQ	DQ11	DQ12	VDDQ	DQ13	DQ14	VSSQ	DQ15	VSS

■ FUNCTIONAL BLOCK DIAGRAM



■ PIN FUNCTION DESCRIPTION

PIN NAME	INPUT	FUNCTION
CLK	System Clock	Active on the positive going edge to sample all inputs
/CS	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK , CKE and L(U)DQM
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior new command. Disable input buffers for power down in standby
A0 ~ A11	Address	Row / column address are multiplexed on the same pins. Row address : RA0~RA11, column address : CA0~CA7
A12, A13	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time. RAS Row Address Strobe
/RAS	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with /RAS low. Enables row access & precharge.
/CAS	Column Address Strobe	Latches column address on the positive going edge of the CLK with CAS low. Enables column access.
/WE	Write Enable	Enables write operation and row precharge. Latches data in starting from /CAS, /WE active.
L(U)DQM	Data Input / Output Mask	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ0 ~ DQ15	Data Input / Output	Data inputs / outputs are multiplexed on the same pins.
VDD / VSS	Power Supply / Ground	Power and ground for the input buffers and the core logic.
VDDQ / VSSQ	Data Output Power / Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
NC	No Connection	This pin is recommended to be left No Connection on the device.

■ SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	A13 A12	A10 /AP	A11 A9~A0	Note
Register	Mode Register set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4,5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4,5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down	Entry		H	L	H	X	X	X	X	X			
					L	V	V	V					
	Exit		L	H	X	X	X	X	X				
Precharge Power Down Mode	Entry		H	L	H	X	X	X	X	X			
					L	H	H	H					
	Exit		L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operating Command (NOP)			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V = Valid , X = Don't Care. H = Logic High , L = Logic Low)

Note: 1. OP Code: Operating Code, A0~A11 & A13~A12: Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state. A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM. The automatical precharge without row precharge of command is meant by “Auto”. Auto/self refresh can be issued only at all banks precharge state.

4. A13~A12: Bank select addresses. If both A13 and A12 are “Low” at read, write, row active and precharge, bank A is selected. If both A13 is “Low” and A12 is “High” at read, write, row active and precharge, bank B is selected. If both A13 is “High” and A12 is “Low” at read, write, row active and precharge, bank C is selected. If both A13 and A12 are “High” at read, write, row active and precharge, bank D is selected If A10/AP is “High” at row precharge, A13 and A12 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command cannot be issued. Another bank read/write command can be issued after the end of burst. New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

■ MODE REGISTER TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	A13~A12	A11~A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	Reserved	Reserved	Reserved	Test Mode		CAS Latency			Burst Type	Burst Length		

Test Mode			CAS Latency				Burst Type		Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Reserved	0	0	1	Reserved	1	Interleave	0	0	1	2	2
1	0	Reserved	0	1	0	2			0	1	0	4	4
1	1	Reserved	0	1	1	3			0	1	1	8	8
			1	0	0	Reserved			1	0	0	Reserved	Reserved
			1	0	1	Reserved			1	0	1	Reserved	Reserved
			1	1	0	Reserved			1	1	0	Reserved	Reserved
			1	1	1	Reserved			1	1	1	Full Page	Reserved

Full Page Length: 256

■ BURST SEQUENCE (BURST LENGTH = 4)

Initial Adrress		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

■ BURST SEQUENCE (BURST LENGTH = 8)

Initial			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

■ DEVICE OPERATIONS

SDRAM BASIC FUNCTION

Three major differences between this SDRAM and conventional DRAMs are: synchronized operation, burst mode, and mode register.

The **synchronized operation** is the fundamental difference. An SDRAM uses a clock input for the synchronization, where the DRAM is basically asynchronous memory although it has been using two clocks, $\overline{RAS}$ and $\overline{CAS}$. Each operation of DRAM is determined by their timing phase differences while each operation of SDRAM is determined by commands and all operations are referenced to a positive clock edge.

The **burst mode** is a very high-speed access mode utilizing an internal column address generator. Once a column addresses for the first access is set, following addresses are automatically generated by the internal column address counter.

The **mode registe**r is to justify the SDRAM operation and function into desired system conditions. MODE REGISTER TABLE shows how SDRAM can be configured for system requirement by mode register programming.

POWER UP & INITIALIZATION SEQUENCE

1.Apply power and start clock, Attempt to maintain CKE = ”H”, DQM = ”H” and the other pin are NOP condition at the inputs.

2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.

3. Issue precharge commands for all banks of the devices.

4. Issue 2 or more auto-refresh (REF) commands.

5. Issue mode register set (MRS) command to initialize the mode register. RFU (Reserved for future use) should stay “0” during this cycle.

Note: 1. It is recommended that DQM and CKE keep track VCC to insure that output is High-Z state.

2. The Mode Register Set command can be set before 2 Auto-refresh commands.

CLOCK (CLK) and CLOCK ENABLE (CKE)

All input and output signals of SDRAM use register type buffers. A CLK is used as a trigger for the register and internal burst counter increment. All inputs are latched by a positive edge of CLK. All outputs are validated by the CLK. CKE is a high active clock enable signal. When CKE = Low is latched at a clock input during active cycle, the next clock will be internally masked. During idle state (all banks have been precharged), the Power Down mode (standby) is entered with CKE = Low and this will make extremely low standby current.

PRECHARGE AND PRECHARGE OPTION (PRE, PALL)

SDRAM memory core is the same as conventional DRAMs’, requiring precharge and refresh operations. Precharge rewrites the bit line and to reset the internal Row address line and is executed by the Precharge command (PRE).

With the Precharge command, SDRAM will automatically be in standby state after precharge time (t_{RP}).

The precharged bank is selected by combination of AP and A_{13}, A_{12} when Precharge command is asserted. If AP = High, all banks are precharged regardless of A_{13}, A_{12} (PALL). If AP = Low, a bank to be selected by A_{12}, A_{13} is precharged (PRE).

The auto-precharge enters precharge mode at the end of burst mode of read or write without Precharge command assertion. This auto precharge is entered by AP = High when a read or write command is asserted.

Enable and disable auto precharge function are controlled by A10/AP in read/write command:

A10/AP	A12	A13	Operating
0	0	0	Disable auto precharge, leave A bank active at end of burst.
	0	1	Disable auto precharge, leave B bank active at end of burst.
	1	0	Disable auto precharge, leave C bank active at end of burst.
	1	1	Disable auto precharge, leave D bank active at end of burst.
1	0	0	Enable auto precharge , precharge bank A at end of burst.
	0	1	Enable auto precharge , precharge bank B at end of burst.
	1	0	Enable auto precharge , precharge bank C at end of burst.
	1	1	Enable auto precharge , precharge bank D at end of burst.

A10/AP and A13~A12 control bank precharge when precharge is asserted:

A10/AP	A12	A13	Precharge
0	0	0	Bank A
0	0	1	Bank B
0	1	0	Bank C
0	1	1	Bank D
1	X	X	All Banks

AUTO-REFRESH (REF)

Auto-refresh uses the internal refresh address counter. The SDRAM Auto-refresh command (REF) generates Precharge command internally. All banks of SDRAM should be precharged prior to the Auto-refresh command. The Auto-refresh command should also be asserted every 16 μs or a total 4096 refresh commands within a 64 ms period.

SELF-REFRESH ENTRY (SELF)

Self-refresh function provides automatic refresh by an internal timer as well as Auto-refresh and will continue the refresh function until cancelled by SELFX.

The Self-refresh is entered by applying an Auto-refresh command in conjunction with CKE = Low (SELF). Once SDRAM enters the self-refresh mode, all inputs except for CKE will be “don’t care” (either logic high or low level state) and outputs will be in a High-Z state. During a self-refresh mode, CKE = Low should be maintained. SELF command should only be issued after last read data has been appeared on DQ.

Note: When the burst refresh method is used, a total of 4096 auto-refresh commands within 4 ms must be asserted prior to the self-refresh mode entry.

SELF-REFRESH EXIT (SELFX)

To exit self-refresh mode, apply minimum t_{CKSP} after CKE brought high, and then the No operation command (NOP) should be asserted within one t_{RC} period. CKE should be held High within one t_{RC} period after t_{CKSP}.

MODE REGISTER SET (MRS)

The mode register of SDRAM provides a variety of different operations. The register consists of four operation fields; Burst Length, Burst Type, CAS latency, and Operation Code. Refer to MODE REGISTER TABLE.

The mode register can be programmed by the Mode Register Set command (MRS). Each field is set by the address line. Once a mode register is programmed, the contents of the register will be held until re-programmed by another MRS command (or part loses power). MRS command should only be issued on condition that all DQ is in Hi-Z.

The condition of the mode register is undefined after the power-up stage. It is required to set each field after initialization of SDRAM.

CHIP SELECT ($\overline{CS}$)

CS enables all commands inputs, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$, and address input. When $\overline{CS}$ is High, command signals are negated but internal operation such as burst cycle will not be suspended. If such a control isn’t needed, CS can be tied to ground level.

COMMAND INPUT ($\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$)

Unlike a conventional DRAM, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ do not directly imply SDRAM operation, such as Row address strobe by $\overline{RAS}$. Instead, each combination of $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ input in conjunction with $\overline{CS}$ input at a rising edge of the CLK determines SDRAM operation.

ADDRESS INPUT (A0 to A11)

Address input selects an arbitrary location of a total of 1,048,576 words of each memory cell matrix. A total of twenty address input signals are required to decode such a matrix. SDRAM adopts an address multiplexer in order to reduce the pin count of the address line. At a Bank Active command (ACTV), twelve Row addresses are initially latched and the remainders of eight Column addresses are then latched by a Column address strobe command of either a Read command (READ or READA) or Write command (WRIT or WRITA).

BANK SELECT (A12, A13)

This SDRAM has four banks and each bank is organized as 1 M words by 16-bit.

Bank selection by A_{13}, A_{12} occurs at Bank Active command (ACTV) followed by read (READ or READA), write (WRIT or WRITA), and precharge command (PRE).

BANK ACTIVATE

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of t_{RCD} (min) from the time of bank activation. t_{RCD} is the internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing t_{RCD} (min) with cycle time of the clock and then rounding of the result to the next higher integer. The SDRAM has four internal banks in the same chip and shares part of the internal circuitry to reduce chip area; therefore it restricts the activation of four banks simultaneously. Also the noise generated during sensing of each bank of SDRAM is high requiring some time for power supplies to recover before another bank can be sensed reliably. t_{RRD} (min) specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by t_{RAS} (min). Every SDRAM bank activate command must satisfy t_{RAS} (min) specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by t_{RAS} (max) and t_{RAS} (max) can be calculated similar to t_{RCD} specification.

DATA INPUTS AND OUTPUTS (DQ0 to DQ15)

Input data is latched and written into the memory at the clock following the write command input. Data output is obtained by the following conditions followed by a read command input:

T_{RAC}: from the bank active command when t_{RCD} (min) is satisfied. (This parameter is reference only.)

T_{CAC}: from the read command when t_{RCD} is greater than t_{RCD} (min). (This parameter is reference only.)

T_{AC}: from the clock edge after t_{RAC} and t_{CAC}.

The polarity of the output data is identical to that of the input. Data is valid between access time (determined by the three conditions above) and the next positive clock edge (t_{OH}).

DATA I/O MASK (DQML/DQMU)

DQML and DQMU are an active high enable input and has an output disable and input mask function. During burst cycle and when DQML/DQMU = High is latched by a clock, input is masked at the same clock and output will be masked at the second clock later while internal burst counter will increment by one or will go to the next stage depending on burst type.

BURST MODE OPERATION AND BURST TYPE

The burst mode provides faster memory access. The burst mode is implemented by keeping the same Row address and by automatic strobe column address. Access time and cycle time of Burst mode is specified as t_{AC}

and t_{CK}, respectively. The internal column address counter operation is determined by a mode register, which defines burst type and burst count length of 1, 2, 4 or 8 bits of boundary. In order to terminate or to move from the current burst mode to the next stage while the remaining burst count is more than 1, the following combinations will be required:

Current Stage	Next Stage	Method (Assert the following command)	
Burst Read	Burst Read	Read Command	
Burst Read	Burst Write	1st Step	Mask Command (Normally 3 clock cycles)
		2nd Step	Write Command after L_{OWD}
Burst Write	Burst Write	Write Command	
Burst Write	Burst Read	Read Command	
Burst Read	Precharge	Precharge Command	
Burst Write	Precharge	Precharge Command	

The burst type can be selected either sequential or interleave mode if burst length is 2, 4 or 8. The sequential mode is an incremental decoding scheme within a boundary address to be determined by count length; it assigns +1 to the previous (or initial) address until reaching the end of boundary address and then wraps round to least significant address (= 0). The interleave mode is a scrambled decoding scheme for A_0 and A_2. If the first access of column address is even (0), the next address will be odd (1), or vice-versa.

When the full burst operation is executed at single write mode, Auto-precharge command is valid only at write operation. The burst type can be selected either sequential or interleave mode. But only the sequential mode is usable to the full column burst. The sequential mode is an incremental decoding scheme within a boundary address to be determined by burst length; it assigns +1 to the previous (or initial) address until reaching the end of boundary address and then wraps round to least significant address (= 0).

Burst Length	Starting Column Address A2 A1 A0	Sequential	Interleave
2	X X 0	0 – 1	0 – 1
	X X 1	1 – 0	1 – 0
4	X 0 0	0 – 1 – 2 – 3	0 – 1 – 2 – 3
	X 0 1	1 – 2 – 3 – 0	1 – 0 – 3 – 2
	X 1 0	2 – 3 – 0 – 1	2 – 3 – 0 – 1
	X 1 1	3 – 0 – 1 – 2	3 – 2 – 1 – 0
8	0 0 0	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7
	0 0 1	1 – 2 – 3 – 4 – 5 – 6 – 7 – 0	1 – 0 – 3 – 2 – 5 – 4 – 7 – 6
	0 1 0	2 – 3 – 4 – 5 – 6 – 7 – 0 – 1	2 – 3 – 0 – 1 – 6 – 7 – 4 – 5
	0 1 1	3 – 4 – 5 – 6 – 7 – 0 – 1 – 2	3 – 2 – 1 – 0 – 7 – 6 – 5 – 4
	1 0 0	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3
	1 0 1	5 – 6 – 7 – 0 – 1 – 2 – 3 – 4	5 – 4 – 7 – 6 – 1 – 0 – 3 – 2
	1 1 0	6 – 7 – 0 – 1 – 2 – 3 – 4 – 5	6 – 7 – 4 – 5 – 2 – 3 – 0 – 1
	1 1 1	7 – 0 – 1 – 2 – 3 – 4 – 5 – 6	7 – 6 – 5 – 4 – 3 – 2 – 1 – 0

FULL COLUMN BURST AND BURST STOP COMMAND (BST)

The full column burst is an option of burst length and available only at sequential mode of burst type. This full column burst mode is repeatedly access to the same column. If burst mode reaches end of column address, then it wraps round to first column address (= 0) and continues to count until interrupted by the news read (READ) /write (WRIT), precharge (PRE), or burst stop (BST) command. The selection of Auto-precharge option is illegal during the full column burst operation except write command at BURST READ & SINGLE WRITE mode.

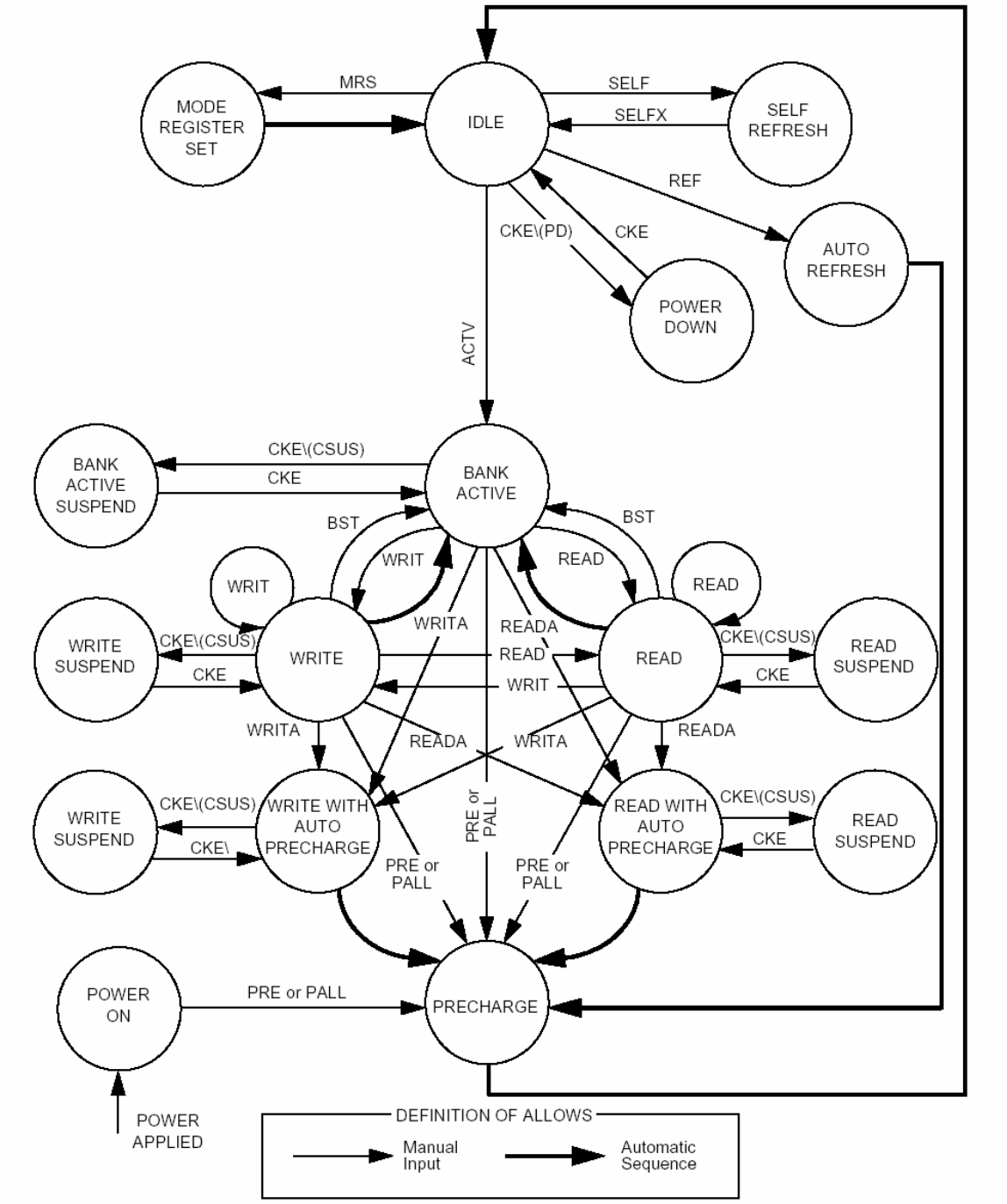
The BST command is applicable to terminate the burst operation. If the BST command is asserted during the burst mode, its operation is terminated immediately and the internal state moves to Bank Active.

When read mode is interrupted by BST command, the output will be in High-Z.

When write mode is interrupted by BST command, the data to be applied at the same time with BST command will be ignored.

Note: When the burst refresh method is used, a total of 4096 auto-refresh commands within 4 ms must be asserted after the self-refresh exit.

■ **STATE DIAGRAM (Simplified for Single BANK Operation State Diagram)**



Note: CKE\ means CKE goes Low-level from High-level.

■ MINIMUM CLOCK LATENCY OR DELAY TIME FOR SINGLE BANK OPERATION

First command \ Second command (same bank)	MRS	ACTV	READ	READA *4	WRITE	WRITEA *4	PRE	PALL	REF	SELF	BST
MRS	t_{RSC}	t_{RSC}					t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}
ACTV			t_{RCD}	t_{RCD}	t_{RCD}	t_{RCD}	t_{RAS}	t_{RAS}			1
READ			1	1	1 *6	1 *6	1 *5	1 *5			1
READA	BL+t_{RP} *1 *2 *3	BL+t_{RP}					BL+t_{RP} *5	BL+t_{RP} *5	BL+t_{RP} *3	BL+t_{RP} *3 *8	
WRITE			t_{WR}	t_{WR}	1	1	t_{DPL} *5	t_{DPL} *5			1
WRITEA	BL-1+ t_{DAL} *3	BL-1+ t_{DAL}					BL-1+ t_{DAL} *5	BL-1+ t_{DAL} *5	BL-1+ t_{DAL} *3	BL-1+ t_{DAL} *3	
PRE	t_{RP} *3 *4	t_{RP}					1	1 *5	t_{RP} *3	t_{RP} *7 *3	1
PALL	t_{RP} *4	t_{RP}					1	1	t_{RP}	t_{RP} *7	1
REF	t_{RC}	t_{RC}					t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}
SELFX	t_{RC}	t_{RC}					t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}

Illegal command

Notes:

*1. BL: Burst length; CL: CAS latency

*2. If t_{RP}(min) ≤ CL × t_{CK}, minimum latency is a sum of (BL + CL) × t_{CK}.

*3. Assume all banks are in Idle state.

*4. Assume output is in High-Z state.

*5. Assume t_{RAS}(min) is satisfied.

*6. Assume no I/O conflict.

*7. Assume after the last data have been appeared on DQ.

*8. If t_{RP}(min) ≤ (CL-1) × t_{CK}, minimum latency is a sum of (BL + CL-1) × t_{CK}.

■ MINIMUM CLOCK LATENCY OR DELAY TIME FOR MULTI BANK OPERATION

First command \ Second command (other bank)	MRS	ACTV	READ *5	READA *5 *6	WRITE *5	WRITEA *5 *6	PRE	PALL	REF	SELF	BST
MRS	t_{RSC}	t_{RSC}					t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}	t_{RSC}
ACTV		t_{RRD} *2	1 *7	1 *7	1 *7	1 *7	1 *6 *7	t_{RAS} *7			1
READ		1 *2 *4	1	1	1 *10	1 *10	1 *6	1 *6			1
READA	BL+t_{RP} *1 *2	1 *2 *4	1 *6	1 *6	1 *6 *10	1 *6 *10	1 *6	BL+t_{RP} *6	BL+t_{RP} *2	BL+t_{RP} *2 *9	
WRITE		1 *2 *4	1	1	1	1	1 *6	t_{DPL} *6			1
WRITEA	BL-1+ t_{DAL} *2	1 *2 *4	1 *6	1 *6	1 *6	1 *6	1 *6	BL-1+ t_{DAL} *6	BL-1+ t_{DAL} *2	BL-1+ t_{DAL} *2	
PRE	t_{RP} *2 *3	1 *2 *4	1 *7	1 *7	1 *7	1 *7	1 *6 *7	1 *7	t_{RP} *2	t_{RP} *8 *2	1
PALL	t_{RP} *3	t_{RP}					1	1	t_{RP}	t_{RP} *8	1
REF	t_{RC}	t_{RC}					t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}
SELFX	t_{RC}	t_{RC}					t_{RC}	t_{RC}	t_{RC}	t_{RC}	t_{RC}

Notes:

*1. If t_{RP}(min) ≤ CL × t_{CK}, minimum latency is a sum of (BL + CL) × t_{CK}.

*2. Assume bank of the object is in Idle state.

*3. Assume output is in High-Z state.

*4. t_{RRD}(min) of other bank (second command will be asserted) is satisfied.

*5. Assume other bank is in active, read or write state.

*6. Assume t_{RAS}(min) is satisfied.

*7. Assume other banks are not in READA/WRITA state.

*8. Assume after the last data have been appeared on DQ.

*9. If t_{RP}(min) ≤ (CL-1) × t_{CK}, minimum latency is a sum of (BL + CL-1) × t_{CK}.

*10. Assume no I/O conflict.

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATING are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

■ DC OPERATING CONDITION

Recommended operating condition s (Voltage referenced to VSS = 0V, TA = 0 to 70 C °)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0		V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	A	3
Output leakage current	I_{OL}	-5	-	5	A	4

Note: 1. $V_{IH(max)}$ = 4.6V AC for pulse width ≤10ns acceptable.

2. $V_{IL(min)}$ = -1.5V AC for pulse width ≤10ns acceptable.

3. Any input 0V ≤V_{IN} ≤V_{DD} + 0.3V, all other pins are not under test = 0V.

4. D_{out} is disabled, 0V ≤V_{OUT} ≤V_{DD}.

■ DC CHARACTERISTICS

Recommended operating condition unless otherwise noted，TA = 0 to 70 C

PARAMETER	SYMBOL	TEST CONDITION	VERSION		UNIT	NOTE
			-6	-7		
Operating Current (One Bank Active)	I_{CC1}	Burst Length = 1, $t_{RC} \geq t_{RC(min)}$, I_{OL} = 0 mA,, tcc = tcc(min)	110	100	mA	1,2
Precharge Standby Current in power-down mode	I_{CC2P}	CKE $\leq V_{IL(max)}$, tcc = tcc(min)	2		mA	
	I_{CC2PS}	CKE & CLK $\leq V_{IL(max)}$, tcc = ∞	1			
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE $\geq V_{IH(min)}$, CS $\leq V_{IH(min)}$, tcc = tcc(min), Input signals are changed one time during 2CLK	20		mA	
	I_{CC2NS}	CKE $\geq V_{IH(min)}$, CLK $\leq V_{IL(max)}$, tcc = ∞ input signals are stable	15			
Active Standby Current in power-down mode	I_{CC3P}	CKE $\leq V_{IL(max)}$, tcc = tcc(min)	10		mA	
	I_{CC3PS}	CKE & CLK $\leq V_{IL(max)}$, tcc = ∞	10			
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE $\geq V_{IH(min)}$, CS $\geq V_{IH(min)}$, tcc = tcc(min), Input signals are changed one time during 2CLK	30		mA	
	I_{CC3NS}	CLK $\leq V_{IL(max)}$, tcc = ∞ input signals are stable	25			
Operating Current (Burst Mode)	I_{CC4}	I_{OL} = 0 mA, Page Burst, All Bank active, Burst Length = 4, CAS Latency = 3	150	140	mA	1,2
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC(min)}$, t_{CC} = tcc(min)	180		mA	
Self Refresh Current	I_{CC6}	CKE $\leq$0.2V	1		mA	

Note: 1. Measured with outputs open.

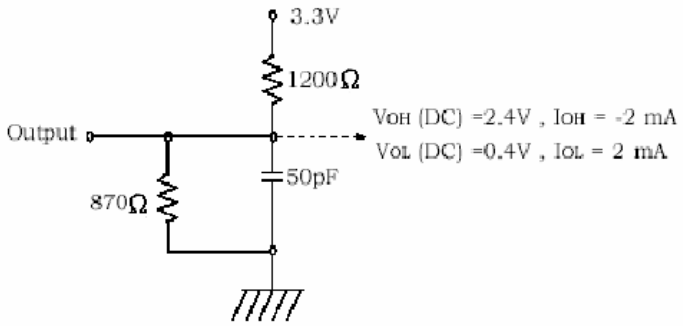
2. Input signals are changed one time during 2 CLKS.

■ CAPACITANCE (VDD = 3.3V, TA = 25 C °, f = 1MHZ)

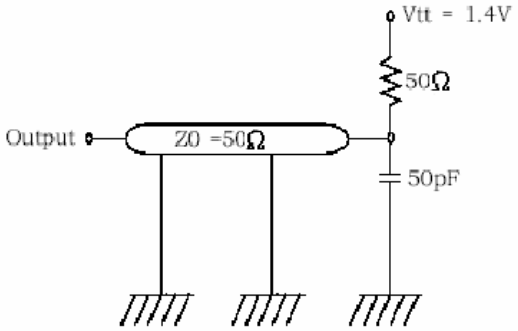
PARAMETER	SYMBOL	MIN	MAX	UNIT
Input capacitance (A0 ~ A11, A13 ~ A12)	C_{IN1}	2	4	Pf
Input capacitance (CLK, CKE, CS , RAS , CAS , WE & L(U)DQM)	C_{IN2}	2	4	Pf
Data input/output capacitance (DQ0 ~ DQ15)	C_{OUT}	2	5	Pf

■ AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V ，TA = 0 to 70 C °)

PARAMETER	VALUE	UNIT
Input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall-time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig.1) DC Output Load Circuit



(Fig.2) AC Output Load Circuit

■ OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

PARAMETER	SYMBOL	VERSION		UNIT	NOTE
		-6	-7		
Row active to row active delay	$t_{RRD(min)}$	12	14	ns	1
/RAS to /CAS delay	$t_{RCD(min)}$	18	20	ns	1
Row precharge time	$t_{RP(min)}$	18	20	ns	1
Row active time	$t_{RAS(min)}$	40	42	ns	1
	$t_{RAS(max)}$	100		ns	
Row cycle time @ Auto refresh	$t_{RC(min)}$	60	70	ns	1,3
Number of valid Output data	CAS latency=3	2		ea	2
	CAS latency=2	1			

Note: 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. In case of row precharge interrupt, auto precharge and read burst stop.

3. A new command may be given t_{RFC} after self refresh exit.

■ AC CHARACTERISTICS (AC operating condition unless otherwise noted)

PARAMATER		SYMBOL	-6		-7		UNIT	NOTE
			MIN	MAX	MIN	MAX		
CLK cycle time	CAS latency = 3	t_{CK}	6	-	7	-	ns	1
	CAS latency = 2		8		10			
CLK to valid output delay	CAS latency = 3	t_{AC}		5.5		6	ns	1, 2
	CAS latency = 2			6		6		
Output data hold time	CAS latency = 3	t_{OH}	2.5				ns	2
	CAS latency = 2		2.5		2.5			
CLK high pulsh width		t_{CH}	2.5		2.5		ns	3
CLK low pulsh width		t_{CL}	2.5		2.5		ns	3
Input setup time		t_{SI}	1.5		1.5		ns	3
Input hold time		t_{HI}	1		1		ns	3
CLK to output in Low-Z		t_{LZ}	0		0		ns	2
CLK to output in Hi-Z	CAS latency = 3	t_{HZ}		5.5		6	ns	
	CAS latency = 2			6		6		
CKE Setup Time for Power Down Exit		t_{CKSP}	1.5		2		ns	4

Note : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns. (tr/2 - 0.5) ns should be considered.

3. Assumed input rise and fall time (tr & tf) =1ns. If tr & tf is longer than 1ns, transient time compensation should be considered.

i.e., [(tr + tf)/2 – 1] ns should be added to the parameter.

4. If input signal transition time (t_T) is longer than 1 ns; [(t_T/2) –0.5] ns should be added to t_{AC} (max), t_{HZ} (max), and t_{CKSP} (min) spec values, [(t_T/2) –0.5] ns should be subtracted from t_{LZ} (min), t_{HZ} (min), and t_{OH} (min) spec values, and (t_T –1.0) ns should be added to t_{CH} (min), t_{CL} (min), t_{SI} (min), and t_{HI} (min) spec values.

■ LATENCY - FIXED VALUES

(The latency values on these parameters are fixed regardless of clock period.)

Parameter		Symbol	CS56ES64163-6T	CS56ES64163-7T	Unit
CKE to Clock Disable		L_{CKE}	1	1	cycle
DQM to Output in High-Z		L_{DQZ}	2	2	cycle
DQM to Input Data Delay		L_{DQD}	0	0	cycle
Last Output to Write Command Delay		L_{OWD}	2	2	cycle
Write Command to Input Data Delay		L_{DWD}	0	0	cycle
Precharge to Output in High-Z Delay	CL = 2	L_{ROH2}	2	2	cycle
	CL = 3	L_{ROH3}	3	3	cycle
Burst Stop Command to Output in High-Z Delay	CL = 2	L_{BSH2}	2	2	cycle
	CL = 3	L_{BSH3}	3	3	cycle
CAS to CAS Delay (min)		L_{CCD}	1	1	cycle
CAS Bank Delay (min)		L_{CBD}	1	1	cycle

■ FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

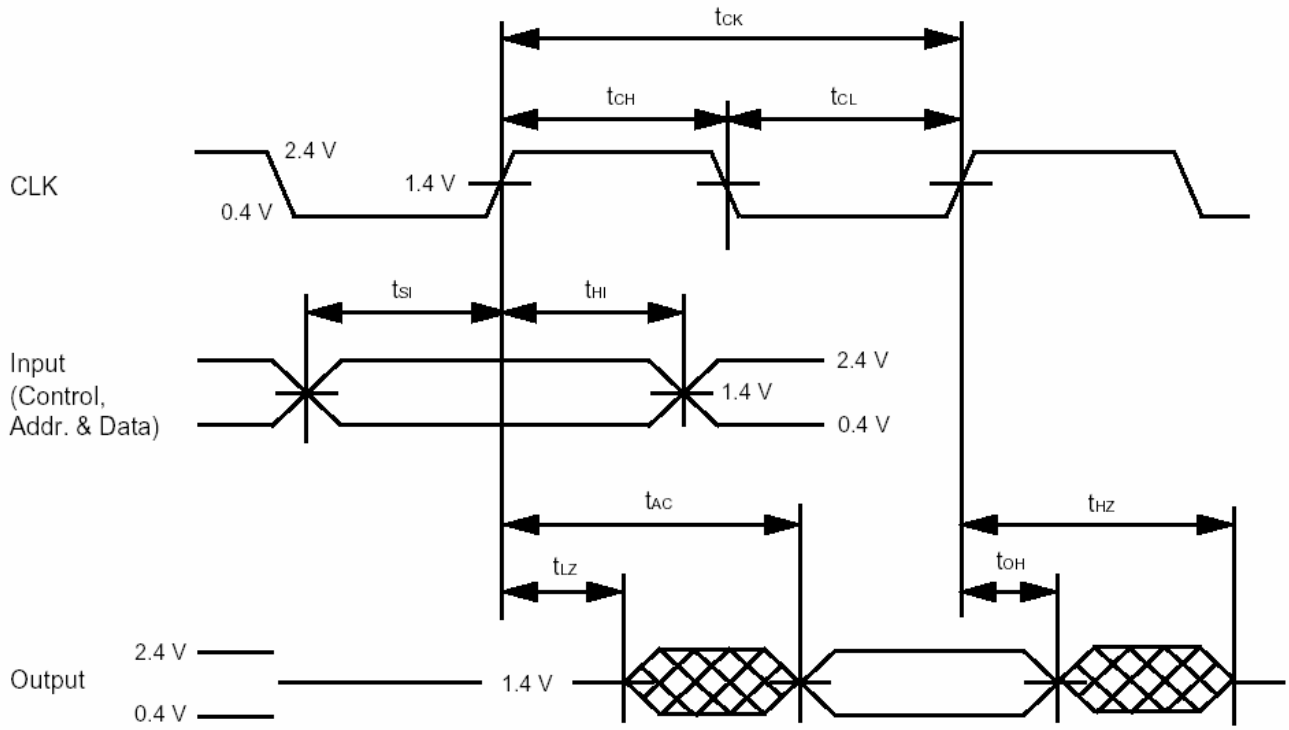
CS56ES64163-6T (Unit : number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		58ns	40ns	18ns	12ns	18ns	6ns	6ns	12ns
166 MHz (6.0ns)	3	10	7	3	2	3	1	1	2
143 MHz (7.0ns)	3	9	6	3	2	3	1	1	2
133 MHZ(7.5ns)	3	8	6	3	2	3	1	1	2
125 MHZ(8.0ns)	2	8	5	3	2	3	1	1	2
100 MHZ(10.0ns)	2	6	4	2	2	2	1	1	2

CS56ES64163-7T (Unit : number of clock)

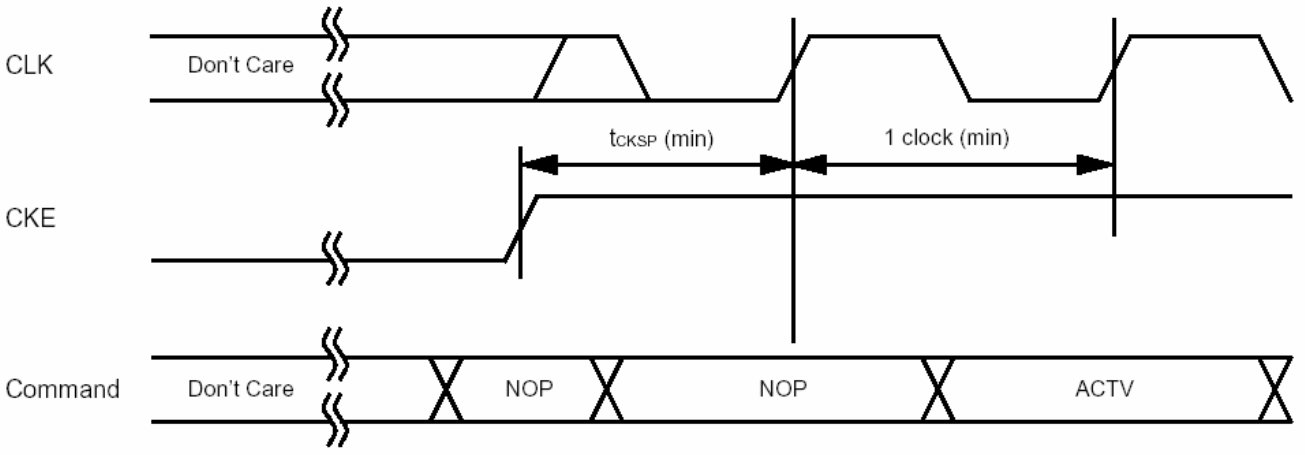
Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		63ns	45ns	20ns	14ns	20ns	7ns	7ns	14ns
143 MHz (6.0ns)	3	9	7	3	2	3	1	1	2
133 MHz (7.0ns)	3	9	6	3	2	3	1	1	2
125 MHZ(7.5ns	3	8	6	3	2	3	1	1	2
100 MHZ(8.0ns)	2	7	5	2	2	2	1	1	2
83 MHZ(10.0ns)	2	6	4	2	2	2	1	1	2

■ TIMING DIAGRAM--SETUP, HOLD AND DELAY TIME

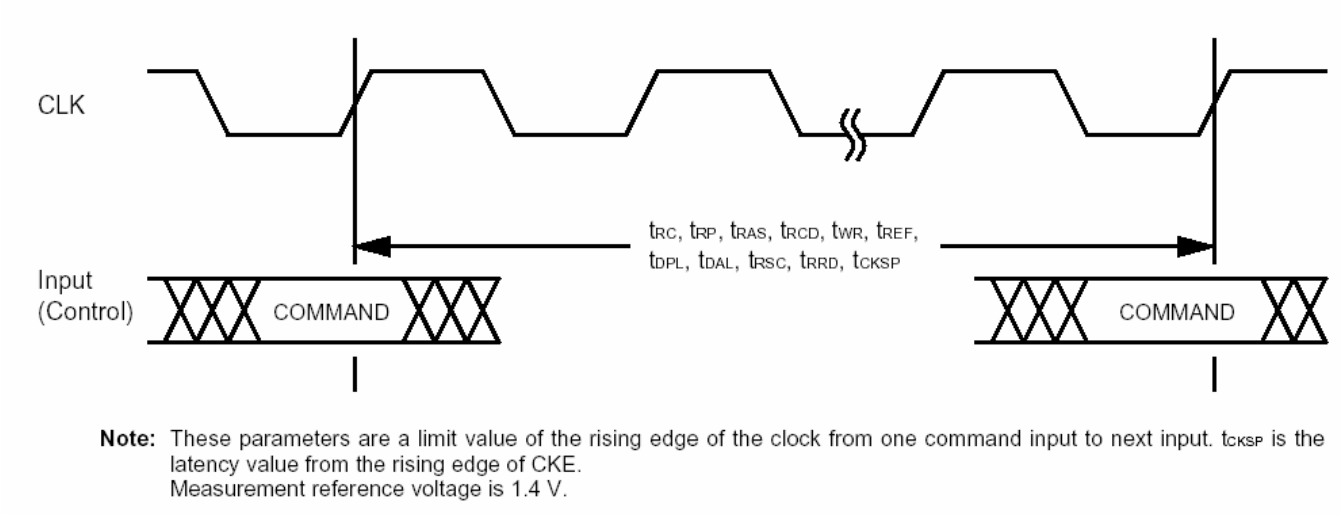


Note: Reference level of input signal is 1.4 V for LVTTL.
Access time is measured at 1.4 V for LVTTL.

■ TIMING DIAGRAM--DELAY TIME FOR POWER DOWN EXIT

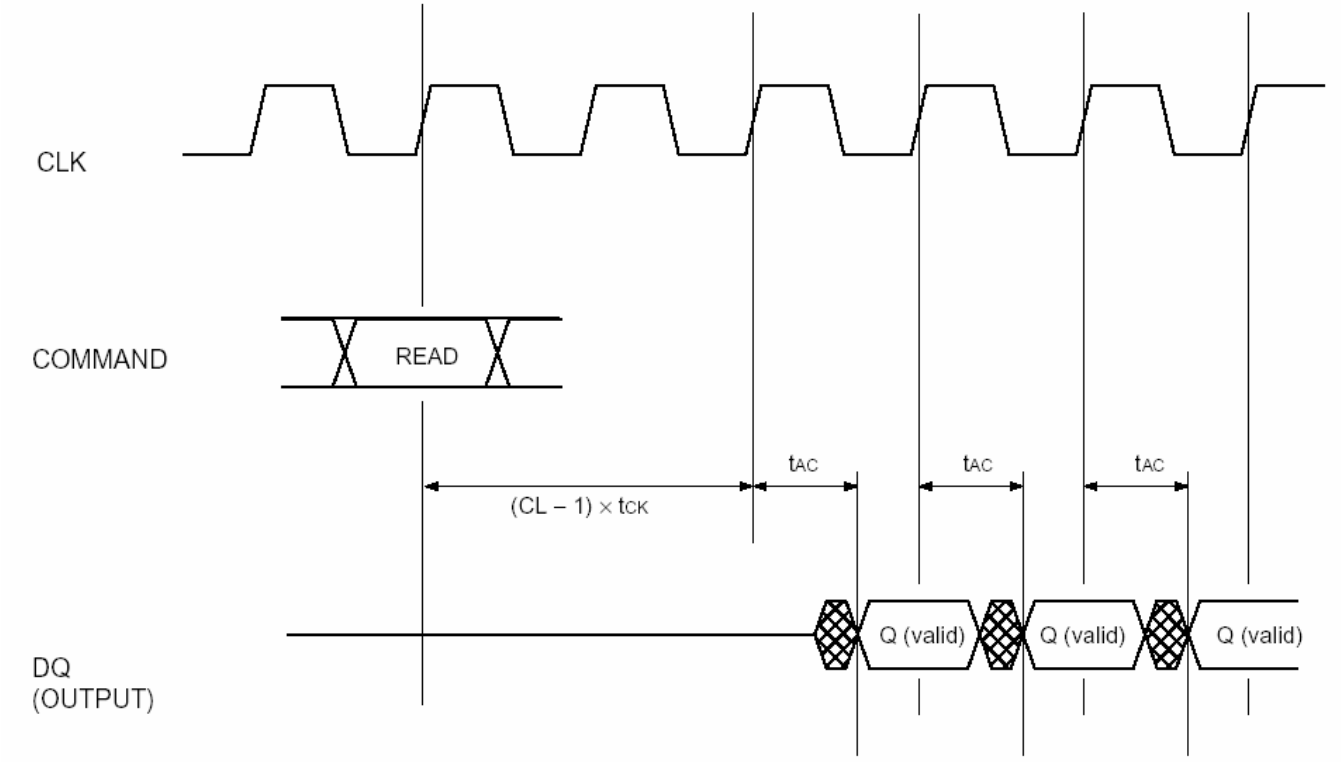


■ TIMING DIAGRAM--PULSE WIDTH

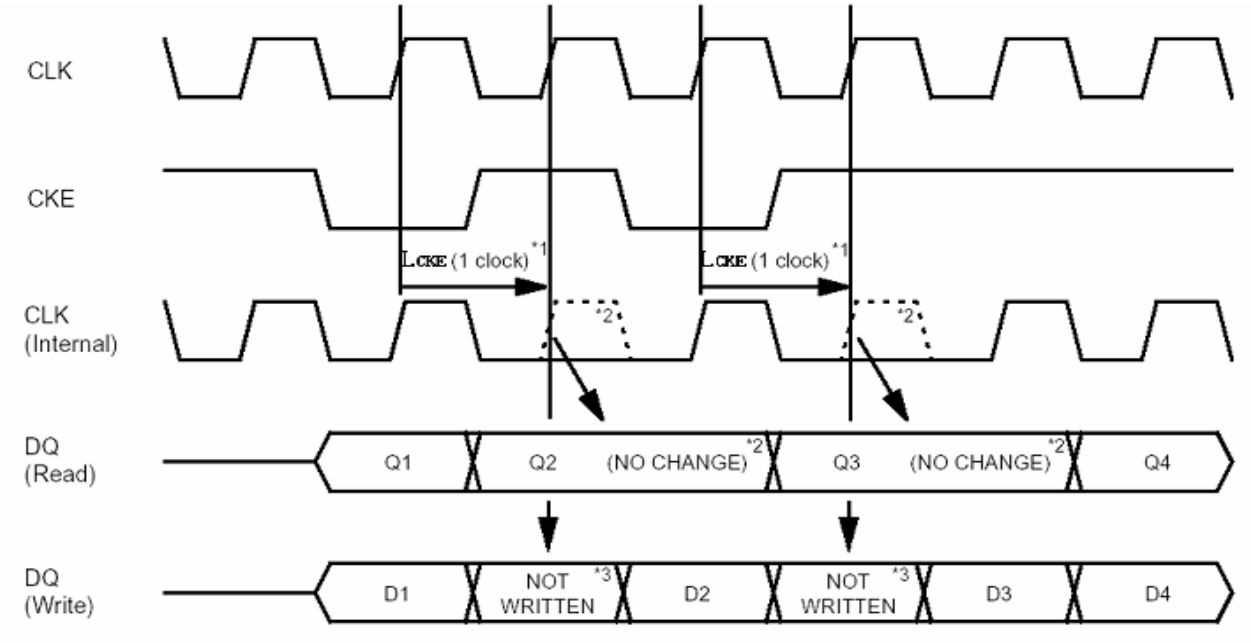


Note: These parameters are a limit value of the rising edge of the clock from one command input to next input. t_{CKSP} is the latency value from the rising edge of CKE.
Measurement reference voltage is 1.4 V.

■ TIMING DIAGRAM--ACCESS TIME



■ TIMING DIAGRAM--CLOCK ENABLE - READ AND WRITE SUSPEND (@ BL = 4)

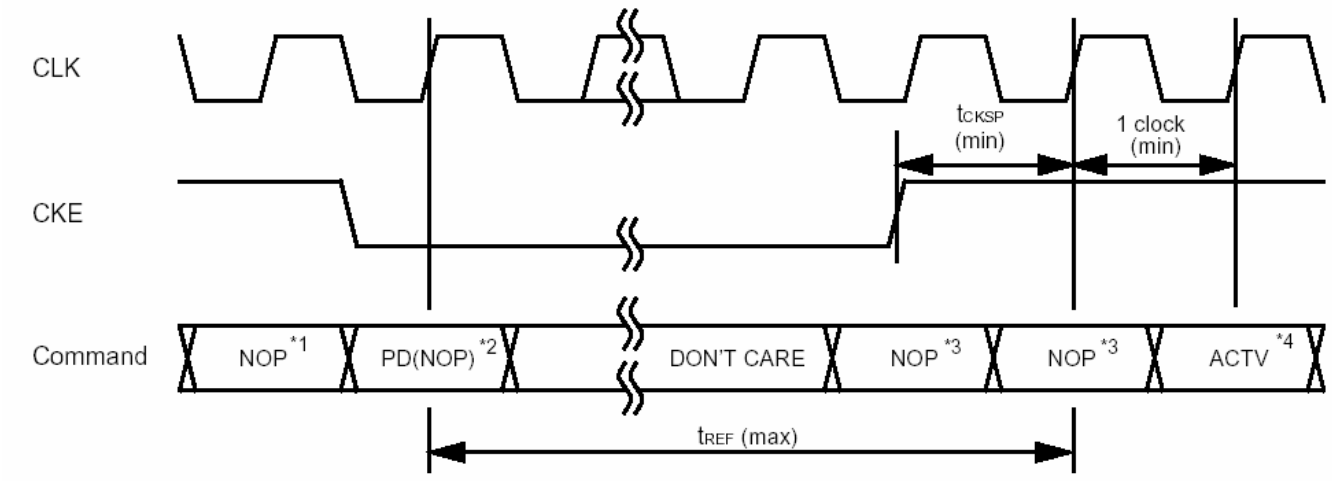


Notes: *1. The latency of CKE (L_{CKE}) is one clock.

*2. During read mode, burst counter will not be incremented/decremented at the next clock of CSUS command. Output data remain the same data.

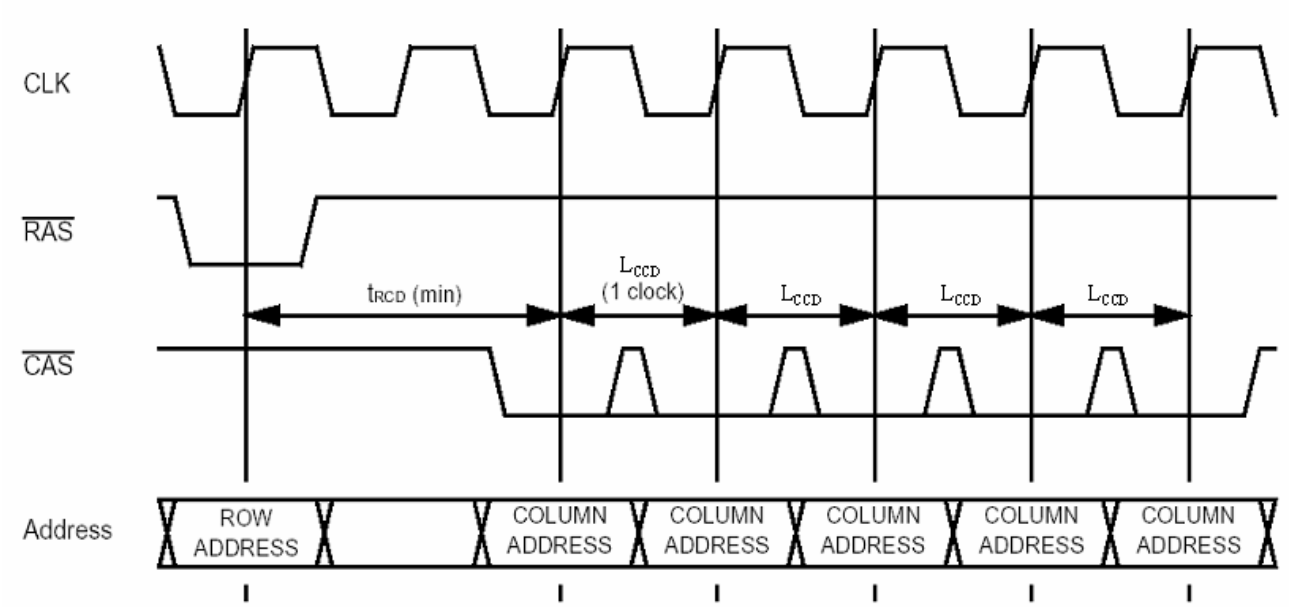
*3. During the write mode, data at the next clock of CSUS command is ignored.

■ TIMING DIAGRAM--CLOCK ENABLE - POWER DOWN ENTRY AND EXIT



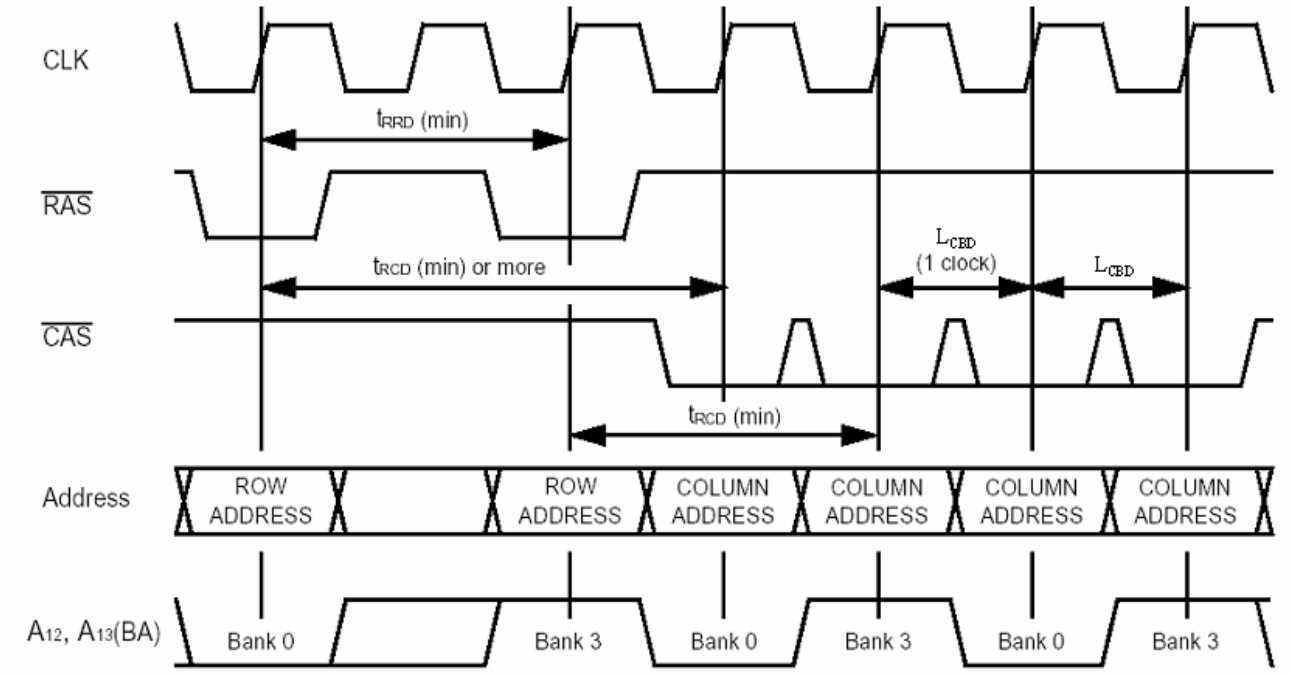
Notes: *1. Precharge command (PRE or PALL) should be asserted if any bank is active and in the burst mode.
*2. Precharge command can be posted in conjunction with CKE after the last read data have been appeared on DQ.
*3. It is recommended to apply NOP command in conjunction with CKE.
*4. The ACTV command can be latched after t_{CKSP} (min) + 1 clock (min).

■ TIMING DIAGRAM--COLUMN ADDRESS TO COLUMN ADDRESS INPUT DELAY



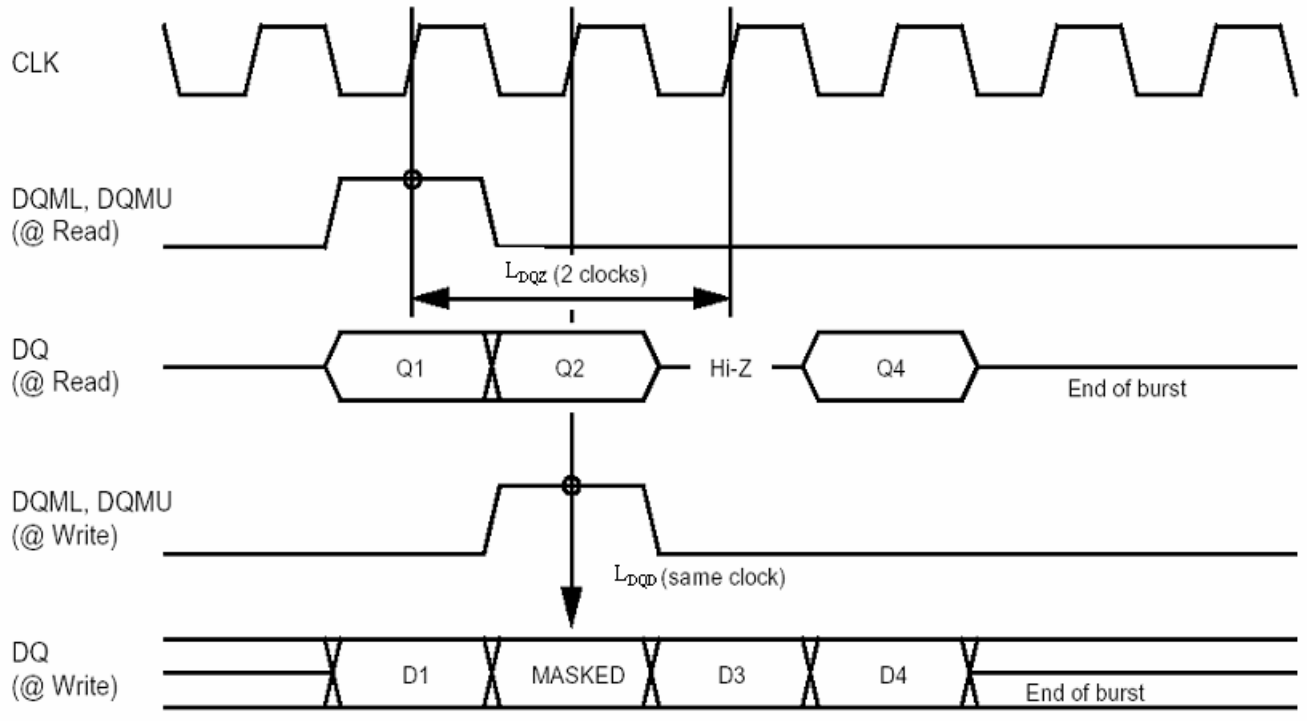
Note: $\overline{CAS}$ to $\overline{CAS}$ delay can be one or more clock period.

■ TIMING DIAGRAM--DIFFERENT BANK ADDRESS INPUT DELAY

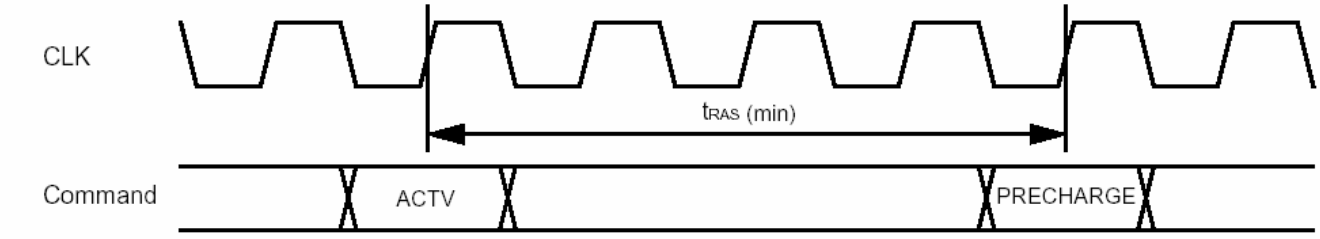


Note: $\overline{CAS}$ Bank delay can be one or more clock period.

■ TIMING DIAGRAM--DQMU, DQML - INPUT MASK AND OUTPUT DISABLE (@ BL = 4)

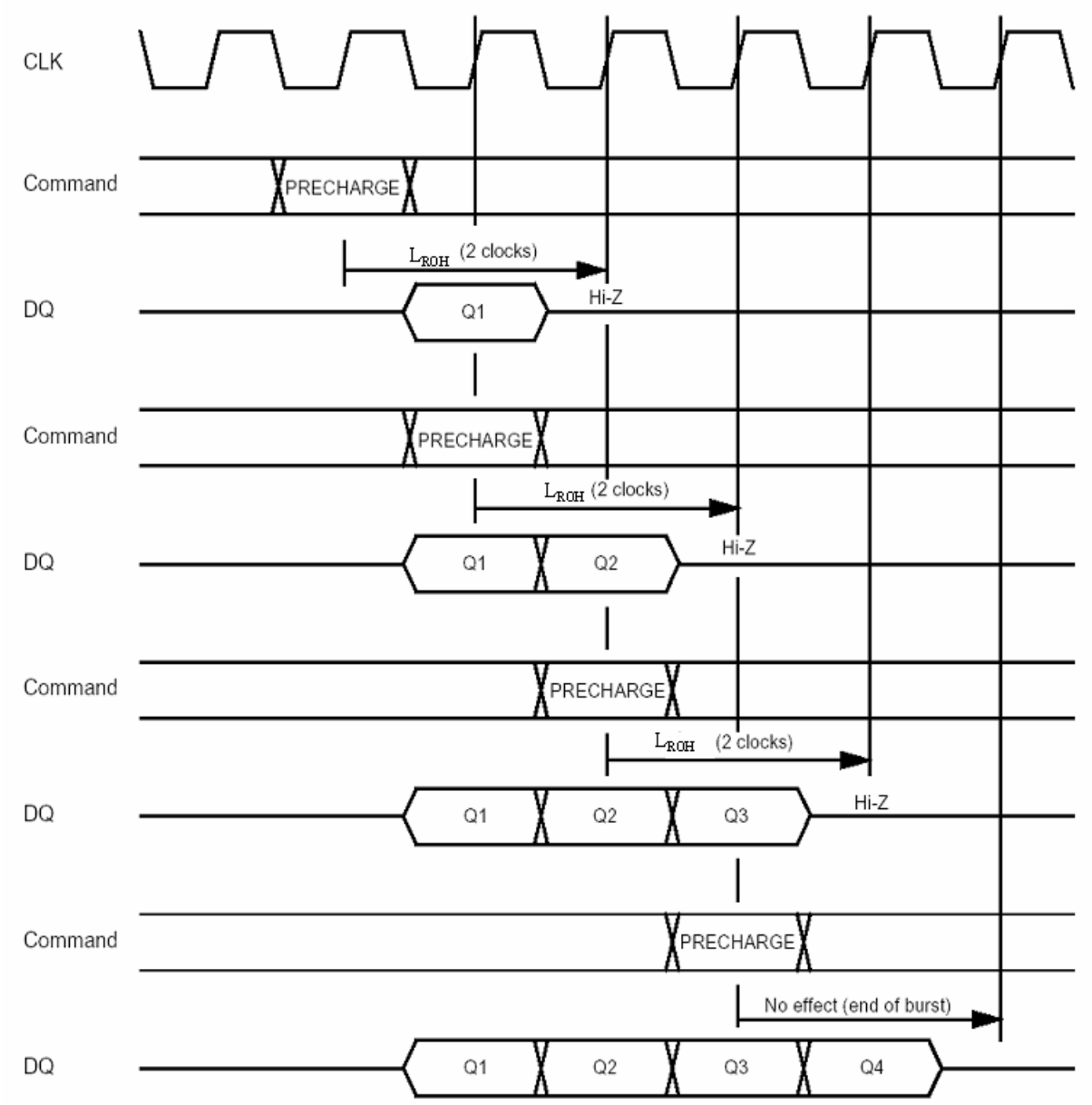


■ TIMING DIAGRAM--PRECHARGE TIMING (APPLIED TO THE SAME BANK)



Note: PRECHARGE means 'PRE' or 'PALL'.

■ **TIMING DIAGRAM--READ INTERRUPTED BY PRECHARGE (EXAMPLE @ CL = 2, BL = 4)**

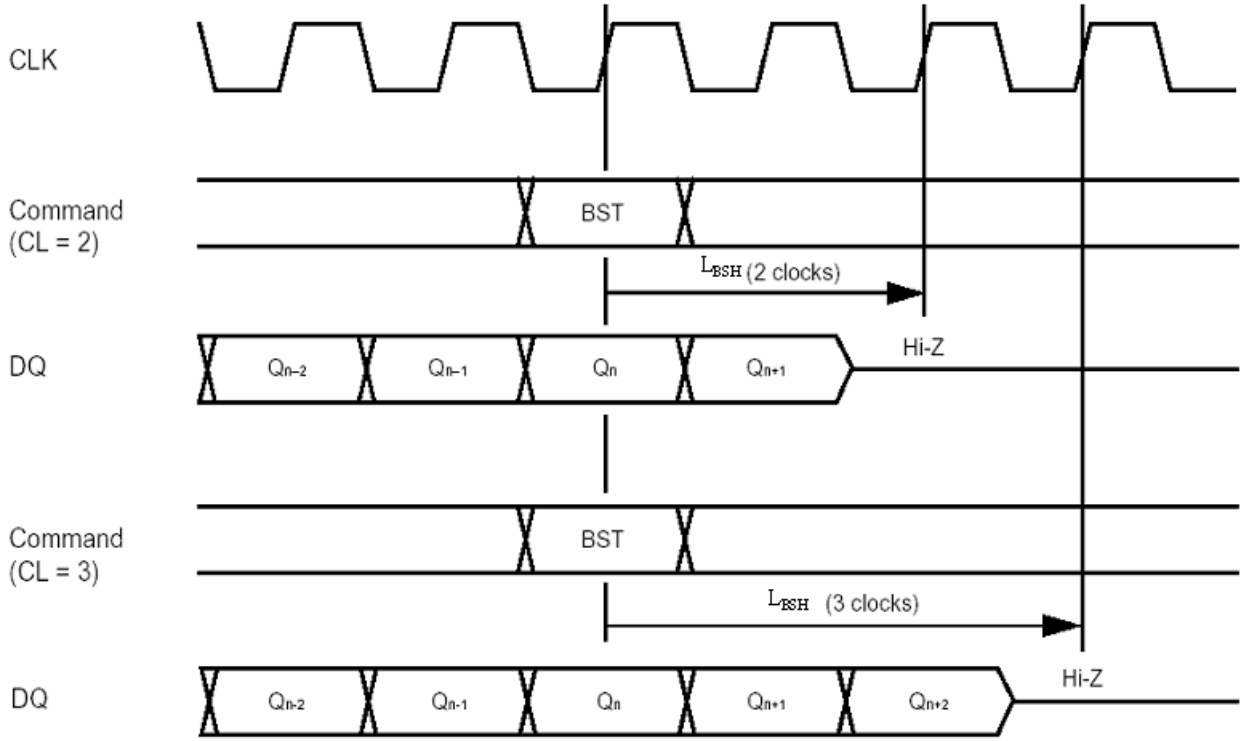


Note: In case of CL = 2, the L_{ROH} is 2 clocks.

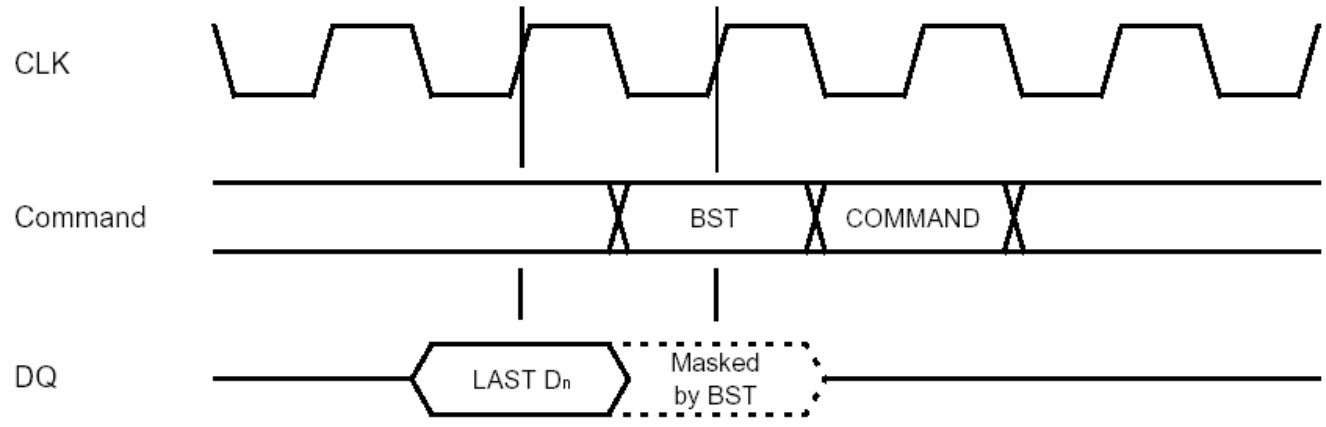
In case of CL = 3, the L_{ROH} is 3 clocks.

PRECHARGE means ‘PRE’ or ‘PALL’.

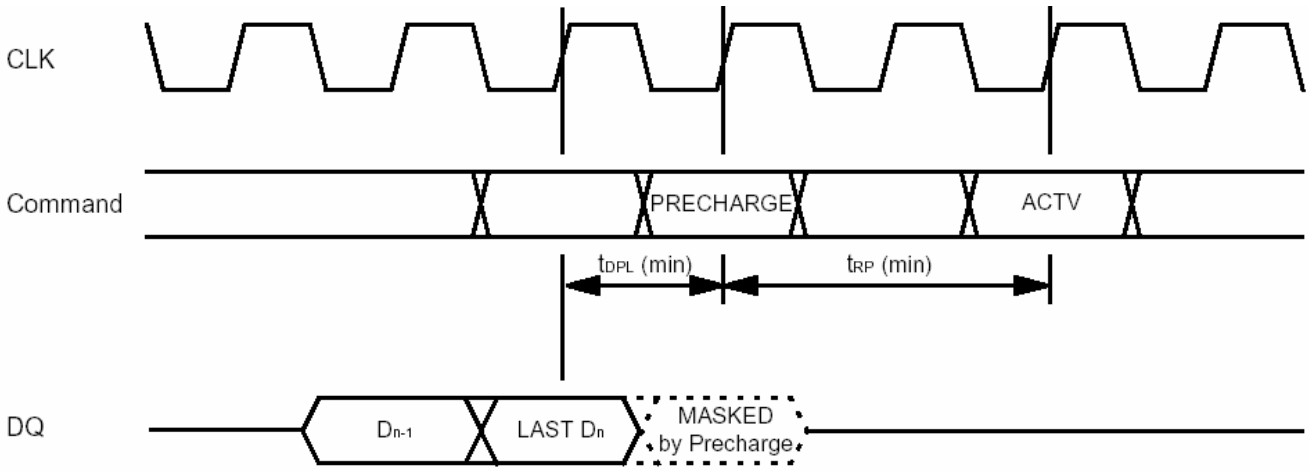
■ **TIMING DIAGRAM--READ INTERRUPTED BY BURST STOP (EXAMPLE @ BL = Full Column)**



■ **TIMING DIAGRAM--WRITE INTERRUPTED BY BURST STOP (EXAMPLE @ CL = 2)**

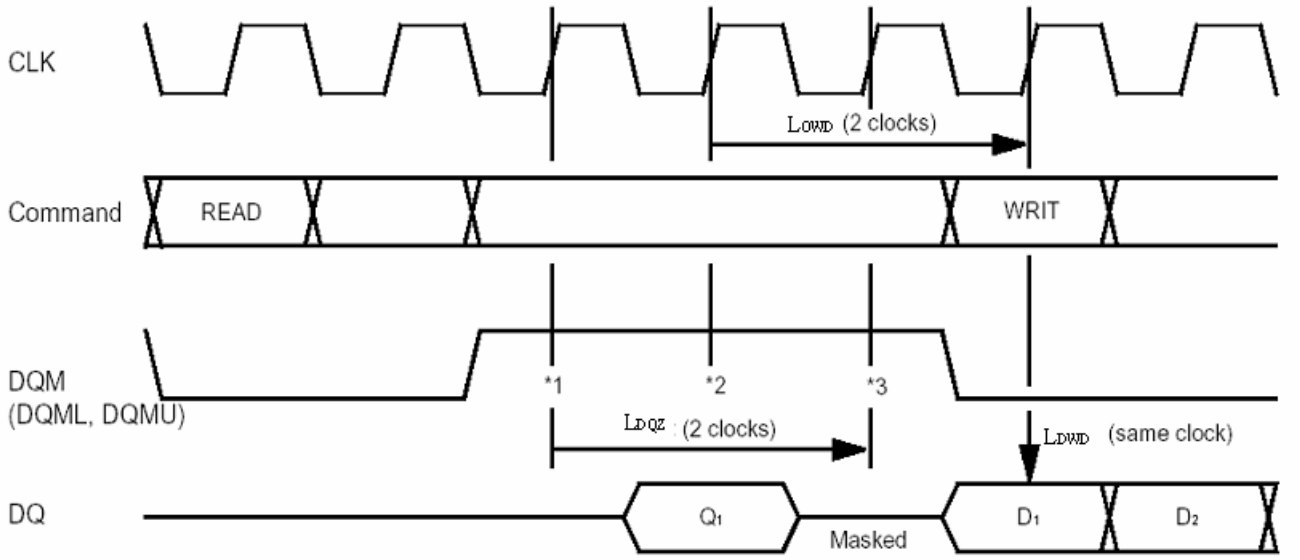


■ TIMING DIAGRAM--WRITE INTERRUPTED BY PRECHARGE (EXAMPLE @ CL = 3)



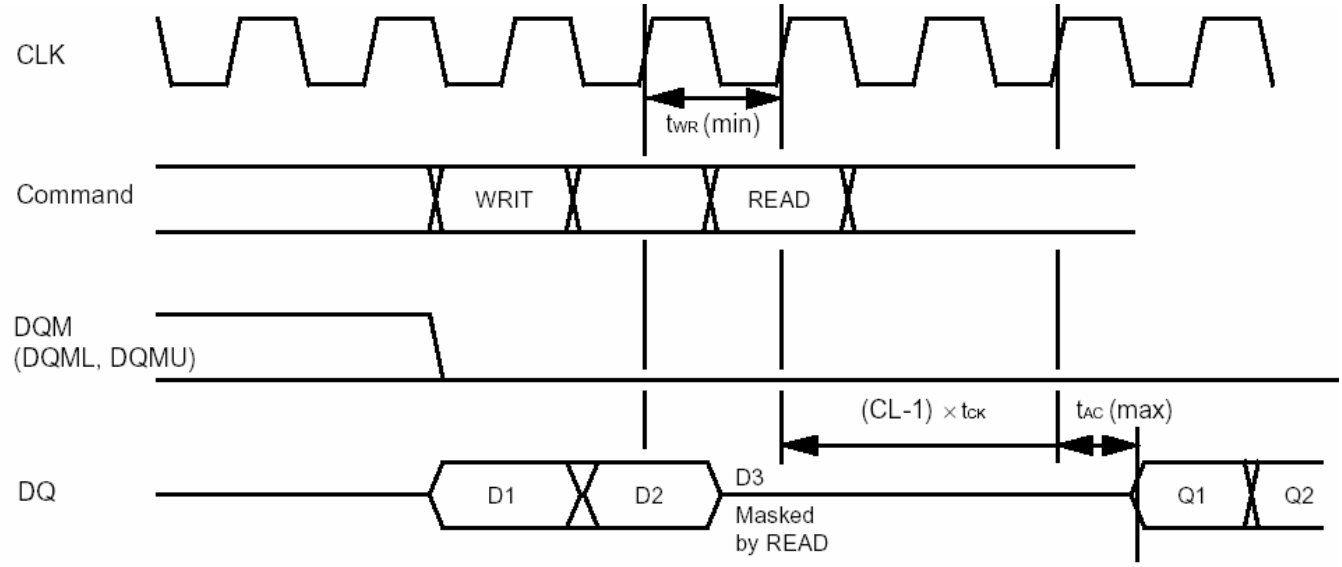
Note: The precharge command (PRE) should only be issued after the t_{DPL} of final data input is satisfied.
PRECHARGE means 'PRE' or 'PALL'.

■ TIMING DIAGRAM--READ INTERRUPTED BY WRITE (EXAMPLE @ CL = 3, BL = 4)



Notes: *1. First DQM makes high-impedance state High-Z between last output and first input data.
*2. Second DQM makes internal output data mask to avoid bus contention.
*3. Third DQM in illustrated above also makes internal output data mask. If burst read ends (final data output) at or after the second clock of burst write, this third DQM is required to avoid internal bus contention.

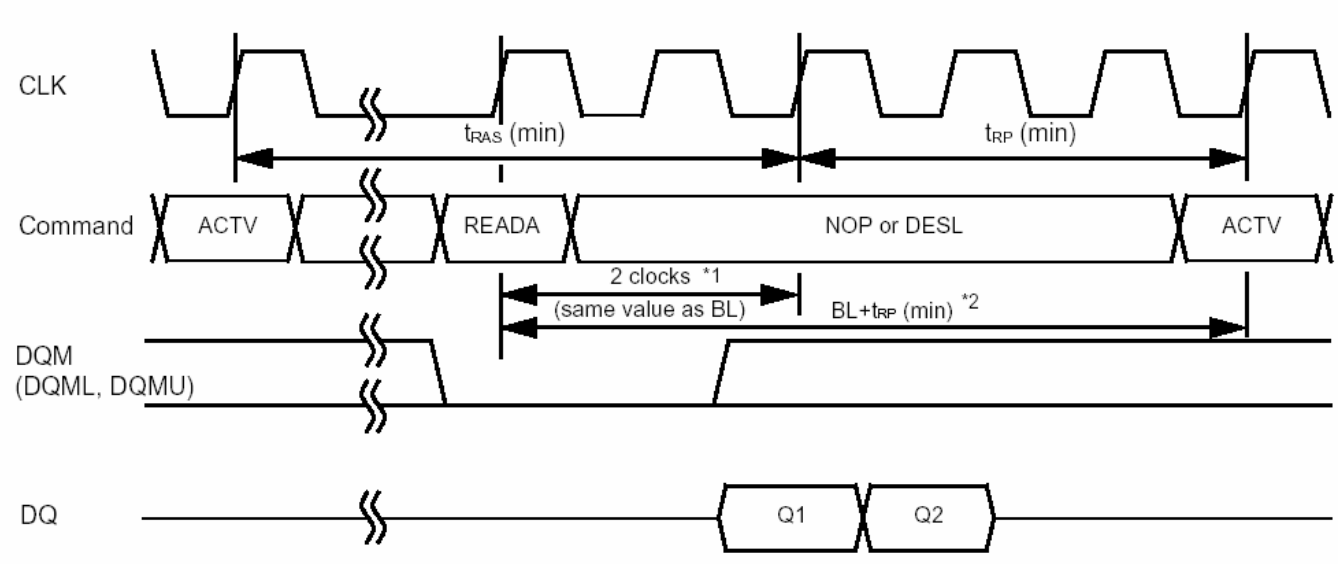
■ TIMING DIAGRAM--WRITE TO READ TIMING (EXAMPLE @ CL = 3, BL = 4)



Note: Read command should be issued after t_{WR} of final data input is satisfied.

■ TIMING DIAGRAM--READ WITH AUTO-PRECHARGE

(EXAPLE @ CL = 2, BL = 2 Applied to same bank)

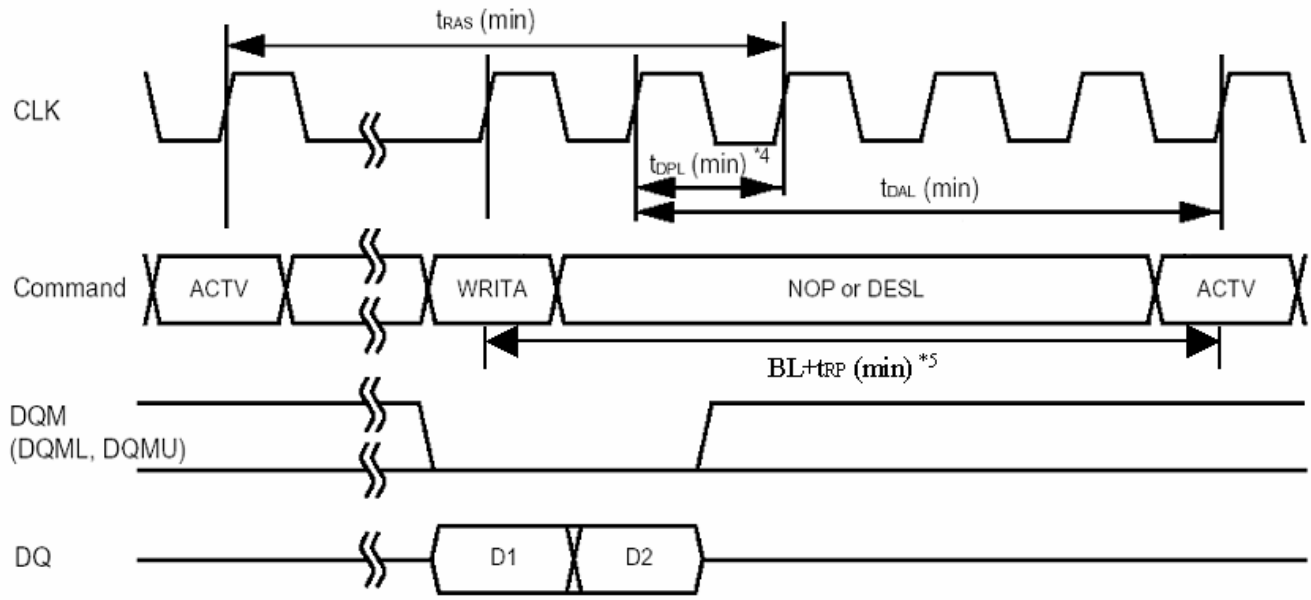


Notes: *1. Precharge at Read with Auto-precharge command (READA) is started from number of clocks that is the same as Burst Length (BL) after the READA command is asserted.

*2. Next ACTV command should be issued after BL+t_{RP} (min) from READA command.

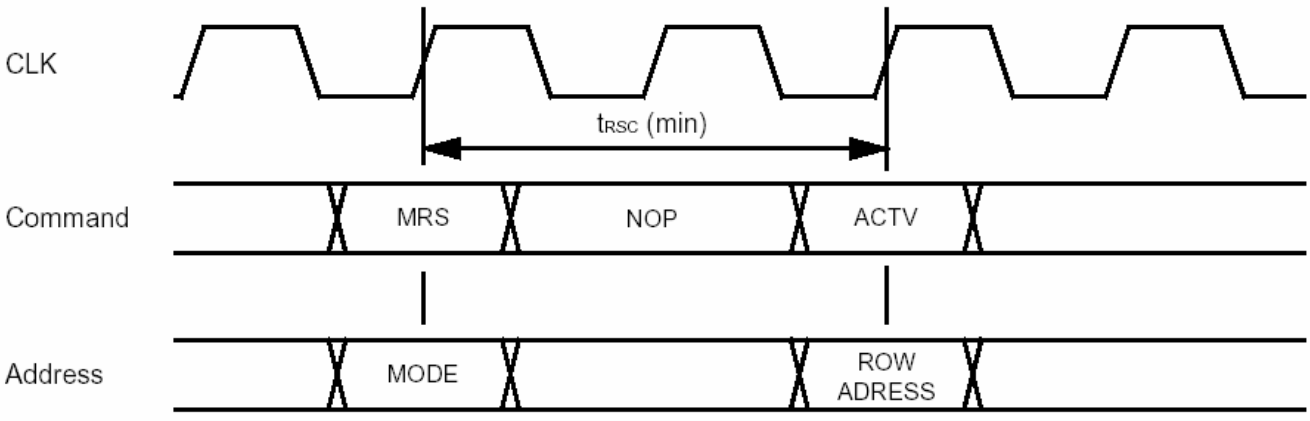
■ TIMING DIAGRAM--WRITE WITH AUTO-PRECHARGE *1, *2, *3

(EXAMPLE @ CL = 2, BL = 2 Applied to same bank)



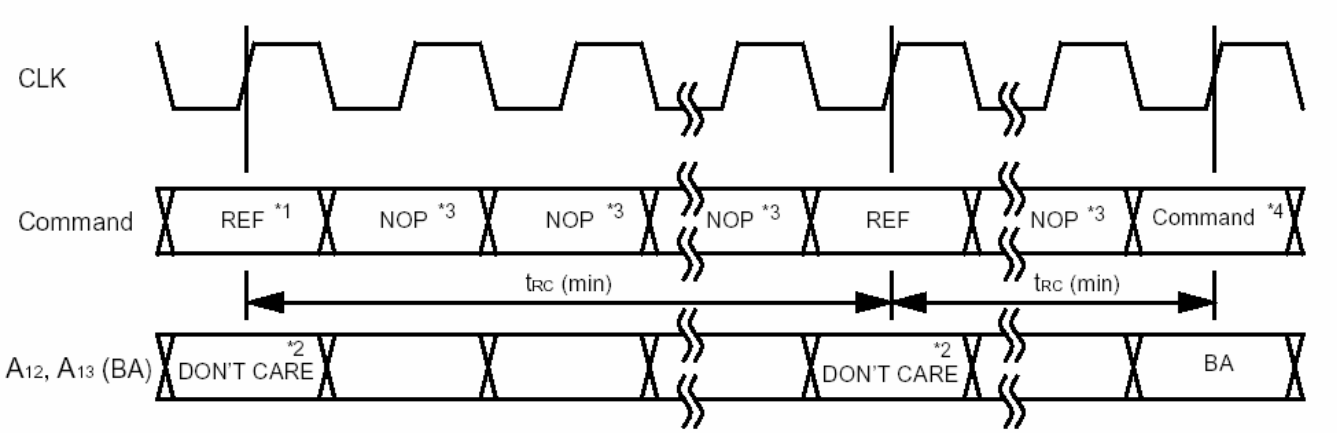
Notes: *1. Even if the final data is masked by DQM, the precharge does not start the clock of final data input.
*2. Once auto precharge command is asserted, no new command within the same bank can be issued.
*3. Auto-precharge command doesn't affect at full column burst operation except Burst READ & Single Write.
*4. Precharge at write with Auto-precharge is started after the t_{DPL} from the end of burst.
*5. Next command should be issued after BL+ t_{RP} (min) at CL = 2, BL+1+t_{RP} (min) at CL = 3 from WRITA command.

■ TIMING DIAGRAM--MODE REGISTER SET TIMING



Note: The Mode Register Set command (MRS) should only be asserted after all banks have been precharged.

■ TIMING DIAGRAM--AUTO-REFRESH TIMING



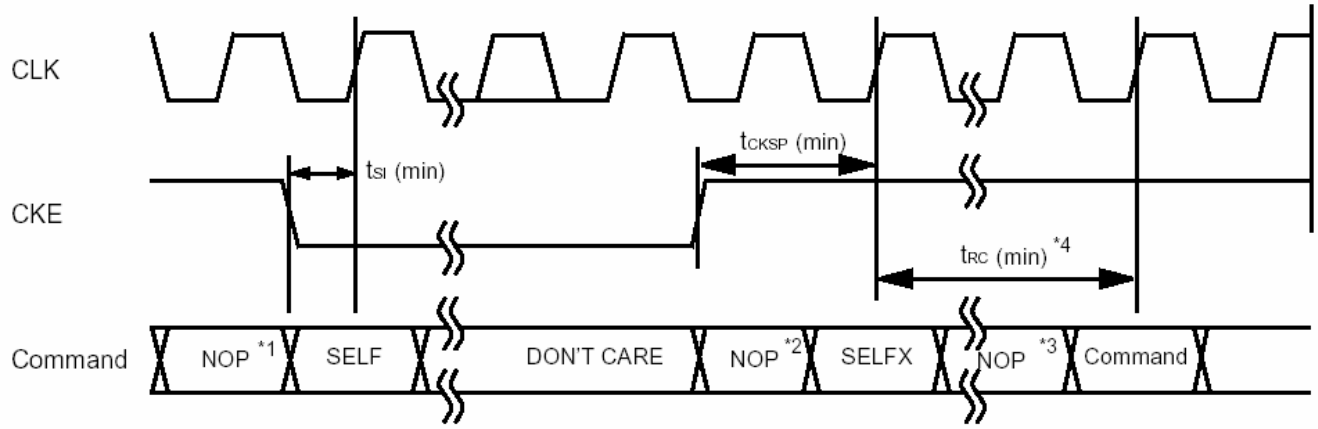
Notes: *1. All banks should be precharged prior to the first Auto-refresh command (REF).

*2. Bank select is ignored at REF command. The refresh address and bank select are selected by internal refresh counter.

*3. NOP command should be asserted during t_{RC} period while Auto-refresh mode.

*4. Any activation command such as ACTV or MRS command other than REF command should be asserted after t_{RC} from the last REF command.

■ TIMING DIAGRAM--SELF-REFRESH ENTRY AND EXIT TIMING



Notes: *1. Precharge command (PRE or PALL) should be asserted if any bank is active prior to Self-refresh Entry command (SELF).

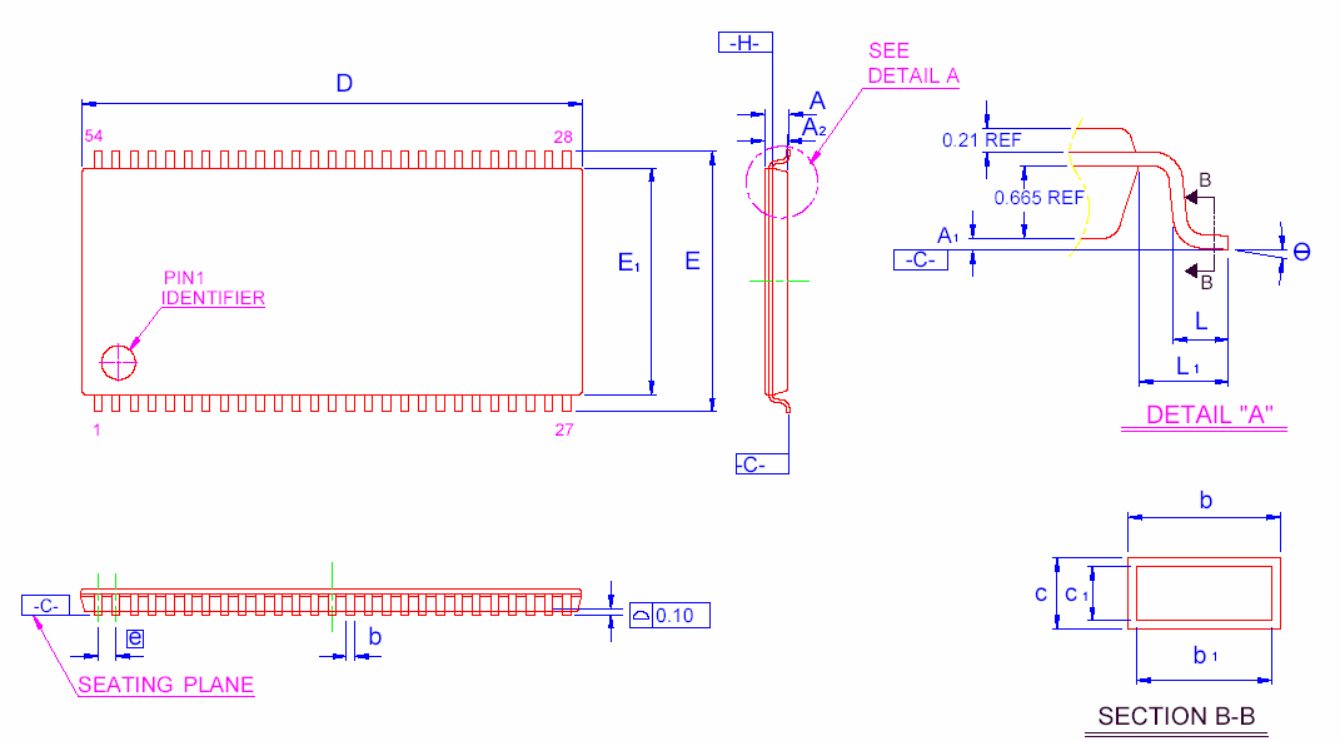
*2. The Self-refresh Exit command (SELFX) is latched after t_{CKSP} (min). It is recommended to apply NOP command in conjunction with CKE.

*3. Either NOP or DESL command can be used during t_{RC} period.

*4. CKE should be held high within one t_{RC} period after t_{CKSP}.

■ PACKING DIMENSIONS

54-LEAD TSOP(II) SDRAM (400mil) (1:3)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	———	———	1.2	———	———	0.047
A1	0.05	0.1	0.15	0.002	0.004	0.006
A2	0.95	1	1.05	0.037	0.039	0.041
b	0.25	———	0.45	0.01	———	0.018
b1	0.25	0.35	0.4	0.01	0.014	0.016
c	0.12	———	0.21	0.005	———	0.008
c1	0.1	0.127	0.16	0.004	0.005	0.006
D	22.22 BSC			0.875 BSC		
E	11.76 BSC			0.463 BSC		
E1	10.16 BSC			0.400 BSC		
L	0.4	0.5	0.6	0.016	0.02	0.024
L1	0.80 REF			0.031 REF		
e	0.80 BSC			0.031 BSC		
Θ	0°	———	10°	0°	———	10°